## IN THE CLAIMS

Cancel Claims 1-6, 12-14 and 16. Re-write Claim 15 as follows.

- 1. (Canceled herewith)
- 2. (Canceled herewith)
- 3. (Canceled herewith)
- 4. (Canceled herewith)
- 5. (Canceled herewith)
- 6. (Canceled herewith)
- 7. (Previously Amended) A method for making an embedded semiconductor memory device comprising:

forming one or more diffusion bit line regions in a semiconductor substrate; then

thermally oxidizing the upper surface of the semiconductor substrate, thereby forming a bottom oxide layer over the upper surface of the semiconductor substrate and simultaneously forming bit line oxide regions over each of the one or more diffusion bit line regions; and then

forming an intermediate dielectric layer over the bottom oxide layer and the bit line oxide regions; and implanting CMOS well regions through the intermediate dielectric layer and the bottom oxide layer in a first region of the semiconductor substrate.

8. (Previously Amended) The method of Claim 7, further comprising:

removing the intermediate dielectric layer and the bottom oxide layer in the first region of the semiconductor substrate; and then

depositing a top dielectric layer over the intermediate dielectric layer and the first region of the semiconductor substrate using a chemical vapor deposition process.

- 9. (Original) The method of Claim 8, further comprising fabricating one or more high-voltage transistors in the first region of the semiconductor substrate, wherein the high-voltage transistors use the top dielectric layer as a gate dielectric layer.
- 10. (Original) The method of Claim 8, further comprising forming a sacrificial oxide layer over the first region of the semiconductor substrate after removing the intermediate dielectric layer and the bottom oxide layer, but before depositing the top dielectric layer
- 11. (Original) The method of Claim 9, further comprising fabricating one or more low-voltage transistors in the first region of the semiconductor substrate, wherein each of the low voltage logic transistors have a gate dielectric layer thinner than the top dielectric layer.
  - 12. (Canceled herewith)
  - 13. (Canceled herewith)
  - 14. (Canceled herewith)
- 15. (Presently Amended) The method of Claim 1, further comprising: A method for making an embedded semiconductor memory device comprising:

forming one or more diffusion bit line regions in a semiconductor substrate; then

thermally oxidizing the upper surface of the semiconductor substrate, thereby forming a bottom oxide layer over the upper surface of the semiconductor substrate and simultaneously forming bit line oxide regions over each of the one or more diffusion bit line regions; then

forming an intermediate dielectric layer over the bottom oxide layer and the bit line oxide regions

depositing a top dielectric layer over the intermediate dielectric layer;

forming a conductive layer over the top dielectric layer;

patterning the conductive layer to define a plurality of word lines that extend over the bit line oxide regions and the bottom oxide layer; and

removing the top dielectric layer and intermediate dielectric layer located between the plurality of word lines.

## 16. (Canceled herewith)